

<b>FORM PTO-1449</b> (REV. 6-89)		U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office		Attorney's Docket No. 21192-06625	Application No. 10/040,852
<b>INFORMATION DISCLOSURE CITATION</b> (Use several sheets if necessary)				Applicant Tommy K. Eng	
				Filing Date December 28, 2001	Group Art Unit 2825

## U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If
TP	A1	5,870,308	02/09/99	Dangelo	395	500.02	
TD	A2	5,572,437	11/05/96	Rostoker <i>et al.</i>	364	489	
TD	A3	5,572,436	11/05/96	Dangelo <i>et al.</i>	364	489	
TD	A4	5,557,531	09/17/96	Rostoker <i>et al.</i>	364	489	
TD	A5	5,555,201	09/10/96	Dangelo <i>et al.</i>	364	489	
TD	A6	5,553,002	09/03/96	Dangelo <i>et al.</i>	364	489	
TD	A7	5,544,067	08/06/96	Rostoker <i>et al.</i>	364	489	
TD	A8	5,544,066	08/06/96	Rostoker <i>et al.</i>	364	489	
TP	A9	5,541,849	07/30/96	Rostoker <i>et al.</i>	364	489	
TP	A10	5,537,580	07/16/96	Giomi <i>et al.</i>	395	500	
TP	A11	5,530,841	06/25/96	Gregory <i>et al.</i>	395	500	
TP	A12	5,526,277	06/11/96	Dangelo <i>et al.</i>	364	489	
TD	A13	5,493,508	02/20/96	Dangelo <i>et al.</i>	364	489	
TD	A14	5,222,030	06/22/93	Dangelo <i>et al.</i>	364	489	

## FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
TD	B1	WO 96/02038	01/25/96	PCT	G06F	17/50		
TD	B2	0 539 641	05/05/93	EP	G06F	15/60		

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TD	C1	Alpert, C. J. <i>et al.</i> , "Quadratic Placement Revisited," Association for Computing Machinery, Inc., Design Automation Conference, pp. 752-757, June 1997.
TD	C2	Dutt, N.D. <i>et al.</i> , "RT Component Sets for High-Level Design Applications," <i>VLSI Design</i> , Gordon & Breach, Switzerland, Vol. 5, No. 2, pp. 155-165, 1997.
TD	C3	Kumar, T. <i>et al.</i> , "Hierarchical Behavioral Partitioning for Multicomponent Synthesis," Proceedings Euro-Dac '96, European Design Automation Conference with Euro-VHDL '96 and Exhibition (CAT No. 96CB36000), pp. 212-217, Los Alamitos, CA., September 1996.
TD	C4	Nair, R. <i>et al.</i> , "Generation of Performance Constraints for Layout," <i>IEEE Transactions on Computer-Aided Design</i> , Vol. 8, No. 8, pp. 860-874, August 1989.
TD	C5	Shahid, Kham, "RTL Floorplanning Speeds Deep-Submicron Design," <i>Computer Design</i> , Vol. 35, No. 2, pp. 103-106, February 1996.

EXAMINER Almundo	DATE CONSIDERED 8/13/03
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EXAMINER: Initial if references considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered.  
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